Zhang Zhenhui

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Gender: Male | Native place: Fuzhou, Fujian

EDUCATION

Xidian University Sep 2019–Jul 2022
Space Engineering | M.E. | Space Science and Technology College Xi'an City
GPA: 4.00/4.00

Civil Aviation University of China Sep 2015–Aug 2019
Communication Engineering | B.E. | Electronic Information and Automation College Tianjin City
GPA: 3.46/4.00

SKILLS/CERTIFICATES

Foreign language: CET-4, PETS-3; Computer: NCRE-2, NCRE-3, NCRE-4; Cartographer: Level 4

PROFESSIONAL SKILLS

-- Proficient in using Vivado software and Verilog hardware description language to develop FPGA devices, master the development process of Xilinx related FPGA and ZYNQ devices and the use of various IPs, and have rich experience in FPGA device design and development;

-- Proficient in the schematic design of various devices, able to independently carry out Multisim, LTspice circuit simulation and Altium Designer, Cadence circuit board design and drawing, with rich experience in circuit design;

-- Familiar with the basic operation of Linux operating system and the development and design process of Petalinux System, master the embedded development of 51 series, Ardrino, STM32 Series MCU;

-- Proficient in using SW, UG and other three-dimensional modeling software, draftsman level 4, able to carry out simple structural design and assembly work;

-- Understand the use of Visual Studio software and the preliminary development of C .

HONORARY AWARDS

National Second Prize/Best object Award of the 7th China Graduate Future Aircraft Contest Nov 2021
People's first/second-class scholarships Sept 2016/Sept 2017/Sept 2019
First Prize of College Students' Engineering Training Comprehensive Ability Competition May 2017
First/Third Prize of National Undergraduate Electronic Design Competition in Tianjin Dec 2017/Dec 2016
"Beidou Cup" Science and Technology Competition National Second/Excellent Prize May 2017/May 2016
Best Idea /Best Hands on Ability Award of Honeywell-Star Jul 2017/Jul 2016
Second Prize of NXP National College Students' Smart Car Competition in North China Aug 2017
First Prize of Tianjin Robot Competition Oct 2016
Second/Third Prize of Robot Competition in North China Nov 2017/ Nov 2016

PROJECT EXPERIENCE

Main control unit of scientific electronic control SPU Dec 2019-Up to Now
-- Shanghai Institute of Optics and precision machinery, Chinese Academy of Sciences Head of Hardware Design

Project Introduction: This controller will be used in the ultracold atomic physics experiment cabinet in the experimental module II "Mengtian" of China space station, which is the main control module in the experimental system. This controller mainly realizes the functions of sending control commands to the laser subsystem and physical control unit, as well as the acquisition and processing of experimental data and images. Several boards are interconnected by VPX structure, and use several zynq ultrascale series FPGAs of Xilinx company as processing and control equipment. The configuration and control instructions required by the laser subsystem and physical

control unit are transmitted through the network, and the experimental images are collected by usb-ccd camera, converted into HDMI signals and output to the display screen. Through the coordination of high-speed ADC, DAC and DDS devices, the laser intensity and frequency are monitored by AOM devices, and then the laser intensity and frequency are adjusted and stabilized by adjusting the output of DAC and DDS devices.

Main Tasks: as the project Hardware Director, complete the schematic drawing of all boards and PCB layout and wiring, including FPGA power supply circuit, PHY circuit, USB circuit; The hardware logic development of zynq device is completed. The user-defined IP based on Axi bus is written in Verilog language, and the axi-dma interconnection IP is added. The high-precision parallel work of multi-channel USB, network port, HDMI display, ADC, DAC, TTL, UART and SPI is realized. In addition, according to the special requirements of the space project, the circuit design and code writing are processed and verified.

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Ultra high speed data acquisition and continuous storage system Jun 2019-May 2020

-- Xi'an Branch of China Academy of space technology FPGA Hardware Development Engineer

Project Description: the system uses two Xilinx virtex7 series FPGAs as the platform, uses two High-Speed ADCs with 5Gsps sampling rate and 8bit data bit width for analog signal sampling, and transmits 80Gbps sampling data to the computer memory for back-end processing in real time through PCIe.

Main work: as a member of the project team, completed the hardware logic development. Two vc709 development boards and four FMC sub boards of DSP 5gsps ADC are used for development and debugging. For a single FPGA development board, idelayer and iserders are used for high-speed data synchronization, and clock edge alignment algorithm is designed to eliminate metastable state; The multi-channel data automatic alignment algorithm is designed for the uneven data; The high-speed LVDS data received by FPGA is recombined with the idea of data splicing; The offset error, gain error and clock phase error of each ADC are eliminated to ensure equal interval sampling; Using MIG IP core to realize the control design of high-speed DDR3 chip, to meet the requirements of high-speed data storage and reading; The asynchronous problem of high speed parallel data transmission across clock domain is eliminated; With the cooperation of members in the same group, Xilinx's DMA for pcieip core is used for the development of high-speed data transmission of pciegen3 to realize 40Gbps stable data transmission and data dropping. Based on the principle of parallel alternating sampling, the clock with different phases is input to the two boards, and the data collected by the two boards are synchronized in the computer to realize the 80gbps data acquisition of the whole system.

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Edge computing based on VITIS AI Mar 2020- Sept 2020

-- Xidian University Project pre-research (Project Manager)

Project Description: Use the VITIS AI tool chain to reduce the complexity of the neural network pre-trained in TensorFlow through the pruning quantizer (DECENT), and convert the Float32 floating-point weights to INT8 fixed-point; then use the neural network compiler (DNNC), Compile the network algorithm to the DPU platform to run efficiently, thereby obtaining a neural network structure that can run efficiently on the ZYNQ platform, and achieve lower power consumption and delay at the edge. In this project, the YOLO3-Tiny network is deployed to the ZCU104 platform to achieve face detection at a resolution of 480*320 or more than 40 frames per second. OpenCV is used for image annotation and display, and the total power consumption of the platform is less than 15W.

PERSONAL SUMMARY

-- Solid foundation, strong thirst for knowledge, rich in team spirit and innovative spirit, practical and serious, have a strong sense of responsibility;

-- FPGA embedded project experience is rich, has a strong research ability, can solve problems independently;

-- Have the ability to write technical documents, good communication and cooperation ability, strong text synthesis and expression ability;